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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,487	11/03/2000	Jean-Didier Allegrucci	003242.P015	7643

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EXAMINER	
MYERS, PAUL R	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,487	ALLEGRUCCI, JEAN-DIDIER	
	Examiner	Art Unit	
	XUAN M. THAI	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to Request for Continued Examination under 37 CFR 1.114 filed on May 13, 2004 with a Preliminary Amendment. Claims 1, 7 and 13 have been amended. Claims 22 and 23 have been added. Claims 1-23 are now pending in the instant application.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of buses must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Jones et al. (USPN 6,356,9609; Jones) and Rieken (USPN 6,665,817).

As per claims 1-2 and 7-8, Jones discloses the claimed invention including a method comprising: recognizing an occurrence of a user-specified event (recognizing control signals being transmitted by external debugging device; see Abstract or CPU executing an event" "instruction or decode special event" col. 8, lines 26-67; col. 9, lines 1-15; col. 11, lines 40-67); generating a signal to cease bus access (issuing instructions to

cease fetching and enter the suspend state; col. 9, lines 15-26; col. 12, lines 12-18) in a configurable system on a chip computer system on integrated chip; Abstract), upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit (CPU0 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44); allowing completion of all pending bus transactions (causes a CPU to drain the execution pipelines; col. 9, lines 35-384 col. 10, lines 15-18); stopping the system clock (stops a11 CPU execution or CPU is suspended; col. 9, lines 23-26) such that the state of the hardware is held static (see col. 9, lines 50-56); and accessing the static state of the hardware through a debug port (debug port 30) (see col. 9, lines 50-55). Jones do not teach a breakpoint unit connected to the internal system bus, such that the breakpoint unit can be programmed through a debug port. Rieken, in the analogous art of debugging in system-on-a-chip system, teaches that it is known to utilize a breakpoint unit connected to internal system bus and capable of being programmed through a debug port (e.g. fig. 5; col. 4, line 50 to col. 5, lines 1-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a breakpoint unit in a debugging environment such as that of Jones and Rieken as taught by Rieken, in that Rieken states that the reprogramming capabilities would allow for a multitude of temporal functions which occur at different times in a product life cycle with the same reprogrammable logic. Hence, the savings in real estate and cost can be achieved (col. 4, lines 18-32).

As per claims 3 and 9, wherein the debug port is a bus master would be within the

teachings of Jones-Rieken in that Jones discloses external debugging device is operable to transmit control signals through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port can be seen as a bus master (Abstract).

As per claims 4 and 10, Jones-Rieken teaches "wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions" (e.g. Jones: col. 9, lines 35-38; Additionally, Rieken teaches the monitoring bus signals: col. 6, lines 1-3).

As per claims 5 and 11, Jones-Rieken teaches "wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions" (e.g. Jones: col. 9, lines 35-38; Additionally, Rieken teaches the generation of a clock freeze cycle: col. 4, lines 9-10 and col. 5, line 1).

As per claims 6 and 12, Jones-Rieken teaches wherein the specified event is programmed by a user (e.g. Jones: col. 12, lines 47-58).

As per claims 13 and 14, Jones discloses the claimed invention including an apparatus comprising: means (event logic 44) to recognize an occurrence of a user-specified event (col. 8, lines 26-67; col. 9, lines 1-15; col. 11, lines 40-67); means (event logic 44; prefetcher 101 and dispatcher 103) to cease bus access (col. 9, lines 15-26; col. 12, lines 12-18) in a configurable system on a chip (computer system on integrated chip; Abstract), upon the occurrence of the user-specified event, the configurable system on a

chip integrating at least a central processing unit (CPU0 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44); means to allow completion of all pending bus transactions (e.g. including event logic 44 causes a CPU to drain the execution pipelines; col. 9, lines 35-38; col. 10, lines 15-18); means to stop the system clock (e.g. including event logic 44, stops all CPU execution or CPU is suspended; col. 9, lines 23-26) such that the state of the hardware is held static (see col. 9, lines 50-56); and means to access the static state of the hardware through a debug port (debug port 30) [e.g. including external debugging device; see col. 9, lines 50-55]. Jones do not teach a breakpoint unit connected to the internal system bus, such that the breakpoint unit can be programmed through a debug port.

Rieken, in the analogous art of debugging in system-on-a-chip system, teaches that it is known to utilize a breakpoint unit connected to internal system bus and capable of being programmed through a debug port (e.g. fig. 5; col. 4, line 50 to col. 5, lines 1-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a breakpoint unit in a debugging environment such as that of Jones and Rieken as taught by Rieken, in that Rieken states that the reprogramming capabilities would allow for a multitude of temporal functions which occur at different times in a product life cycle with the same reprogrammable logic. Hence, the savings in real estate and cost can be achieved (col. 4, lines 18-32).

As per claim 15, Jones-Rieken teaches wherein the debug port is a bus master would be within the teachings of Jones in that Jones discloses external debugging device

is operable to transmit control signals through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port can be seen as a bus master (Abstract).

As per claim 16, Jones-Rieken teaches wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions (e.g. Jones: col. 9, lines 35-38; Additionally, Rieken teaches the monitoring bus signals: col. 6, lines 1-3).

As per claim 17, Jones-Rieken teaches wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions (e.g. Jones: col. 9, lines 35-38; Additionally, Rieken teaches the generation of a clock freeze cycle: col. 4, lines 9-10 and col. 5, line 1).

As per claim 18, Jones-Rieken teaches wherein the specified event is programmed by a user (e.g. Jones: col. 12, lines 47-58).

As per claims 19-21, Jones-Rieken teaches wherein the user-specified event comprises a sequence of events (e.g. see Jones: cols. 9-12).

Response to Arguments

6. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record do not teach or suggest a breakpoint unit connected to a plurality of buses such that the breakpoint unit generates a signal in response to a user-specified event on any of the plurality of buses. Claim 23 is dependent from claim 22, hence it is also allowable for the same reasons.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

XUAN M. THAI
Primary Examiner
Art Unit 2111

XMT